IN THE CLAIMS:

Please cancel Claims 1-24, and add new Claims 25-48, as listed in the following list of claims, which will replace all prior versions, and listings, of the claims in the application:

25. (New) A computer system including a circuit board, the computer system comprising:

a first slot and a second slot coupled to the circuit board, the first slot including a first connector and the second slot including a second connector, the first and second connectors each configured for connecting to a plurality of signal lines;

a hot swap controller connected to the circuit board, the hot swap controller comprising a first means for switching a first plurality of switches, a second means for driving and monitoring signal lines connected to connectors of the first slot and the second slot, and a third means for storing a status information of the signal lines;

standby circuitry removably connected to the hot swap controller, the standby circuitry comprising a fourth means for switching a second plurality of switches, and a fifth means for maintaining the signal lines according to stored status information of the signal lines received from the hot swap controller,

wherein, during a normal operation of the hot swap controller, the first means turns on the first plurality of switches such that the second means monitors and drives ones of the signal lines and the fourth means turns off the second plurality of switches, and during a standby operation of the hot swap controller, the fifth means maintains a status of the signal lines according to the status information stored in the fifth means without monitoring the status of the signal lines, such that when normal operation of the hot swap controller is restored, prior status of the signal lines is recoverable from the standby circuitry.

26. (New) The computer system of Claim 25, wherein the hot swap controller includes a first communication control circuit, the second means connected to the first plurality of switches and to the first means, the first means connected to activation terminals of the first switches via a first control line for switching the first plurality of switches, the communication control circuit connected to the first means, and the connectors for the signal lines connected to the second means through respective ones of the first plurality of switches.

27. (New) The computer system of Claim 26, wherein the fifth means is connected to the second plurality of switches and to the fourth means, the fourth means is connected to respective activation terminals of the second switches via a second control line for switching the second plurality of switches, the fourth means having a communication link with the first communication control circuit, and the connectors for the signal lines connected to the fifth means through respective ones of the second plurality of switches.

28. (New) The computer system of Claim 25, wherein the first means includes an arbitration control circuit, the second means includes a core control circuit, and the third means includes a first register.

29. (New) The computer system of Claim 25, wherein the fourth means includes a second communication control circuit, the fifth means includes a second register.

30. (New) The computer system of Claim 27, wherein the communication link connecting the first communication control circuit and the fourth means comprises an asynchronous communication link.

31. (New) The computer system of Claim 27, wherein the communication link connecting the first communication control circuit and the fourth means comprises a synchronous communication link.

32. (New) The computer system of Claim 26, wherein during every programmed interval of the normal operation, the status of selected ones of the signal lines connected to connectors are transmitted from the first communication control circuit to the fourth means and stored in the fifth means.

33. (New) The computer system of Claim 26, wherein the first communication control circuit is connected to the first means via a plurality of control lines.

34. (New) The computer system of Claim 25, wherein the first means is connected to the second means via a plurality of control lines.

35. (New) The computer system of Claim 25, wherein the fourth means is connected to the fifth means via a plurality of signal lines.

36. (New) A hot swappable computer system including a circuit board, the circuit board having a slot with a first connector for connecting to signal lines of a plug-in card, the computer system comprising:

a hot swap controller connected to a circuit board of the computer system, the hot swap controller comprising a core control circuit including a first register, a plurality of first switches, a first communication control circuit, and an arbitration control circuit, the core control circuit connected to the plurality of first switches and the arbitration control circuit, the arbitration control circuit connected to the first communication control circuit and to activation terminals of the first switches via a common control line, the core control circuit configured to monitor a status of at least one of the signal lines and to alert a CPU of the computer system when a change in the status occurs;

standby circuitry connected to the hot swap controller, the standby circuitry comprising having a second register, a plurality of second switches, and a second communication control circuit, the second register connected to the second switches and the second communication control circuit, the second communication control circuit connected to respective activation terminals of the second switches via a common control line and to the first communication control circuit via a communication link,

wherein during a normal operation of the hot swap controller, the hot swap controller monitors and drives the signal lines, and during a backup operation of the hot swap controller, the standby circuitry maintains a status of the respective signal lines in the second register without monitoring the signal lines, such that when normal operation of the hot swap controller is restored, prior status of the signal lines is recoverable from the standby circuitry.

37. (New) The computer system of Claim 36, wherein the communication link connecting the first and second communication control circuits comprises an asynchronous communication link.

38. (New) The computer system of Claim 36, wherein the communication link connecting the first and second communication control circuits comprises a synchronous communication link.

39. (New) The computer system of Claim 36, wherein at programmed intervals of the normal operation, the status of the signal lines connected to the first through third connector-pins are transmitted from the first communication control circuit to the second communication control circuit and stored in the second register.

40. (New) The computer system of Claim 36, wherein the arbitration control circuit is connected to the first communication control circuit via a plurality of control lines.

41. (New) The computer system of Claim 36, wherein the arbitration control circuit is connected to the core control circuit via a plurality of control lines.

42. (New) The computer system of Claim 36, wherein the second communication control circuit is connected to the second register via a plurality of signal lines.

43. (New) Standby circuitry for use with a hot swap controller to enable hot-swapping of the hot-swap controller in a computer system that comprises a circuit board having slots for plug-in cards of the system, the standby circuitry comprising:

a plurality of switches, respective ones of the plurality of switches configured for switching a connection to individual terminals of at least one computer system slot, wherein the individual terminals are designated for determining status of a plug-in card;

a register configured for storing status information of the terminals, and connected to the plurality of switches; and

a communication control circuit connected to the register, the communication control circuit connected to respective activation terminals of the switches and having a common control line for switching the plurality of switches;

wherein the standby circuitry is configured such that, when the communication control circuit is commanded to turn on the switches prior to beginning standby operation of the hot swap controller, the register thereafter maintains the terminals in a predetermined state according to the status stored in the register without monitoring the terminals of the computer system slot, until normal operation of the hot swap controller is restored.

44. (New) The standby circuitry of Claim 43, further comprising a port for a serial communication link to the hot swap controller.

45. (New) The standby circuitry of Claim 43, wherein the terminals of the computer system slot comprise designated terminals under a CPCI standard selected from the group consisting of BD_SELECT, BD_RESET and BD_HEALTHY.

46. (New) The standby circuitry of Claim 43, wherein the plurality of switches are connected to the individual terminals for a plurality of slots of the computer system, wherein at least some of the individual terminals are designated for determining a status of a respective plug-in card.

47. (New) The standby circuitry of Claim 43, further comprising a port for a communication link to the hot swap controller that is separate from the circuit board of the computer system.

48. (New) The standby circuitry of Claim 43, wherein the standby circuitry is configured to maintain status terminals of a CPCI system in a state predetermined by the hot swap controller while the hot swap controller is taken off-line.